IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

QUICKCOMPILE IP, LLC,	)
	)
Plaintiff,	)
	) Civil Action No. _____
v.	)
	) **JURY TRIAL DEMANDED**
XILINX, INC.,	)
	)
Defendant.	)
	)

COMPLAINT

For its Complaint, Plaintiff QuickCompile IP, LLC ("QuickCompile"), by and through the undersigned counsel, alleges as follows:

THE PARTIES

1. QuickCompile is a Texas limited liability company with a place of business located at 1400 Preston Road, Suite 479, Plano, Texas 75093.

2. Defendant Xilinx, Inc. is a Delaware corporation with, upon information and belief, a place of business located at 5801 Tennyson Parkway, Suite 460, Plano, Texas 75024.

3. Upon information and belief, Defendant has registered with the Texas Secretary of State to conduct business in Texas.

JURISDICTION AND VENUE

4. This action arises under the Patent Act, 35 U.S.C. § 1 *et seq.*

5. Subject matter jurisdiction is proper in this Court under 28 U.S.C. §§ 1331 and 1338.

6. Upon information and belief, Defendant conducts substantial business in this forum, directly or through intermediaries, including: (i) at least a portion of the infringements

alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct and/or deriving substantial revenue from goods and services provided to individuals in this district.

7. Venue is proper in this district pursuant to §§ 1391(b), (c) and 1400(b).

THE PATENTS-IN-SUIT

8. On July 4, 2006, United States Patent No. 7,073,158 (the "'158 patent"), entitled "Automated System For Designing And Developing Field Programmable Gate Arrays" was duly and lawfully issued by the U.S. Patent and Trademark Office. A true and correct copy of the '158 patent is attached hereto as Exhibit A.

9. The claims of the '158 patent provide an inventive concept and do not claim an abstract idea and. The inventive concept of the '158 patent greatly enhances and facilitates the specialized programming of a field-programmable gate array (FPGA), such that source code of high-level programming language designed to process data vectors is mapped onto logic components of an FPGA. The use of high-level programming language to program an FPGA is an improvement over the prior art in that it reduces time and complexity of programming the FPGA.

10. The claims of the '158 patent, moreover, do not merely recite the performance of a longstanding business practice on a computer; rather the claims describe a solution necessarily rooted in computer technology to solve a problem specifically arising in the realm of programming FPGAs. The patent specification, for example, explains how the adoption of FPGAs was slowed by the difficulty in translating desired user-defined algorithms into hardware and the difficulty of updating those algorithms once they are in hardware. The '158 patent overcame these difficulties by simplifying the development of an algorithm or other sequence of

desired operations into the bitstream coding required to program FPGAs.

11. The dependent claims of the '158 patent add additional limitations demonstrating that they also contain inventive concepts, are not directed to any abstract ideas, and do no preempt all ways of programming FPGAs. Claims 4-5 and 7-8, for example, contain specific limitations relating to determining the relative timing between vector processing and identifying the orders and dependencies of vector operands.

12. On September 8, 2009, United States Patent No. 7,587,699 (the "'699 patent"), entitled "Automated System For Designing And Developing Field Programmable Gate Arrays" was duly and lawfully issued by the U.S. Patent and Trademark Office. A true and correct copy of the '699 patent is attached hereto as Exhibit B.

13. The claims of the '699 patent provide an inventive concept and do not claim an abstract idea and. The inventive concept of the '699 patent greatly enhances and facilitates the specialized programming of a FPGA, such that source code of high-level programming language designed to process data vectors is mapped onto logic components of an FPGA. The use of high-level programming language to program an FPGA is an improvement over the prior art in that it reduces time and complexity of programming the FPGA.

14. The claims of the '699 patent, moreover, do not merely recite a computer performing a longstanding business practice; rather the claims describe a solution necessarily rooted in computer technology to solve a problem specifically arising in the realm of programming FPGAs. The patent specification, for example, explains how the adoption of FPGAs was slowed by the difficulty in translating desired user-defined algorithms into hardware and the difficulty of updating those algorithms once they are in hardware. The '699 patent overcame these difficulties by simplifying the development of an algorithm or other sequence of

desired operations into the bitstream coding required to program FPGAs.

15. The dependent claims of the '699 patent add additional limitations demonstrating that they also contain inventive concepts, are not directed to any abstract ideas, and do no preempt all ways of programming FPGAs. Claims 2 and 4-5, for example, contain specific limitations relating to determining the relative timing between vector processing and identifying the orders and dependencies of vector operands.

16. QuickCompile is the assignee and owner of the right, title and interest in and to the '158 and '699 patents, including the right to assert all causes of action arising under said patents and the right to any remedies for their infringement.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,073,158

17. QuickCompile repeats and realleges the allegations of paragraphs 1 through 16 as if fully set forth herein.

18. Without license or authorization and in violation of 35 U.S.C. § 271(a), Defendant has infringed and continues to infringe at least claims 1, 4-5 and 7-8 of the '158 patent by making, using, importing, offering for sale, and/or selling software for programming field programmable gate arrays ("FPGAs"), including, but not limited to Xilinx Vivado High-Level Synthesis ("HLS").

19. More specifically and upon information and belief, Vivado HLS accepts algorithms specified in source code of high level languages, such as C, and C++, *see* http://www.xilinx.com/products/design-tools/vivado/integration/esl-design.html (last accessed May 21, 2015), and it supports processing data vectors. *See* Introduction to FPGA Design with Vivado High-Level Synthesis at 42 (available at http://www.xilinx.com/support/documentation/sw_manuals/ug998-vivado-intro-fpga-design-

hls.pdf (last accessed May 21, 2015)); *see also* Zynq-7000 All Programmable SoC Accelerator for Floating-Point Matrix Multiplication using Vivado HLS at 2 (available at http://www.xilinx.com/support/documentation/application_notes/xapp1170-zynq-hls.pdf (last accessed May 21, 2015)). The Vivado HLS compiler analyzes the input source code and identifies vector processing operations. *See* Introduction to FPGA Design with Vivado High-Level Synthesis at 32 (available at http://www.xilinx.com/support/documentation/sw_manuals/ug998-vivado-intro-fpga-design-hls.pdf (last accessed May 21, 2015)); *see also* Vivado Design Suite User Guide: High-Level Synthesis at 85, 87 (available at http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug902-vivado-high-level-synthesis.pdf (last accessed May 21, 2015)). It maps the vector processing operations onto the hardware resources of an FPGA. *See* Zynq-7000 All Programmable SoC Accelerator for Floating-Point Matrix Multiplication using Vivado HLS at 3 (available at http://www.xilinx.com/support/documentation/application_notes/xapp1170-zynq-hls.pdf (last accessed May 21, 2015)); *see also see also* Vivado Design Suite User Guide: High-Level Synthesis at 7 (available at http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug902-vivado-high-level-synthesis.pdf (last accessed May 21, 2015)); Introduction to FPGA Design with Vivado High-Level Synthesis at 51 (available at http://www.xilinx.com/support/documentation/sw_manuals/ug998-vivado-intro-fpga-design-hls.pdf (last accessed May 21, 2015)). The Vivado HLS outputs a hardware design, which is used to program an FPGA with the user's algorithm. *See* Vivado Design Suite User Guide: High-Level Synthesis at 5, 12, 13 (available at

http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug902-vivado-high-level-synthesis.pdf (last accessed May 21, 2015)); *see also* Zynq-7000 All Programmable SoC Accelerator for Floating-Point Matrix Multiplication using Vivado HLS at 3 (available at http://www.xilinx.com/support/documentation/application_notes/xapp1170-zynq-hls.pdf (last accessed May 21, 2015)).

20. On October 4, 2006, the U.S. Patent and Trademark Office issued an Office Action to Defendant rejecting claims 1-18 of Defendant's U.S. Patent Application No. 10/989,679 under 35 U.S.C. § 102(e) as being anticipated by the '158 patent.

21. On December 19, 2006, Defendant filed an Amendment in Response to First Office Action regarding U.S. Patent Application No. 10/989,679, where it presented arguments with respect to the '158 patent.

22. Defendant has had knowledge of the '158 patent since at least as of the date it received the October 4, 2006 Office Action.

23. Thus, Defendant has been on notice of the '158 patent since, at the latest, the date it received the October 4, 2006 Office Action.

24. Upon information and belief, Defendant infringed and continues to infringe the '158 patent despite its knowledge of the '158 patent and Defendant's infringement has been objectively reckless and willful.

25. In particular, Defendant's customers' and end-users' use of Defendant's products and services which use programmed FPGAs, such as programmed FPGAs with Vivado HLS, is facilitated by the use of methods patented under the '158 patent. Thus, Defendant's customers and end-users are able to program a FPGA by accepting a user-defined algorithm specified in a source code of a high level language and designed to process

data vectors with one, two, or more dimensions; analyze the user-defined algorithm, including identifying the vector processing operations of the source code; map the vector processing operations onto logic components of an FGPA; and program the FPGA with the user-defined algorithm based on the mapping of the logic components.

26. On information and belief, in order to generate profits and revenues, Defendant markets and promotes, e.g., through its website and sales personnel, the use of its products that infringe the '158 patent when used as intended by Defendant's customers and end-users. Defendant further instructs its customers and end-users how to use such products in a manner that infringes the '158 patent (e.g., through on-line technical documentation, instructions, and technical support).

27. In particular, Defendant instructs its customers and end-users through at least on-line support documentation over the Internet how to program an FPGA using the methods patented under the '158 patent. In Vivado HLS, Defendant instructs its customers and end-users through at least on-line support documentation over the Internet how to program a FPGA by accepting a user-defined algorithm specified in a source code of a high level language and designed to process data vectors with one, two, or more dimensions; analyze the user-defined algorithm, including identifying the vector processing operations of the source code; map the vector processing operations onto logic components of an FGPA; and program the FPGA with the user-defined algorithm based on the mapping of the logic components.

28. Defendant still further makes such products accessible to its customers and end-users via the Internet, thus enabling and encouraging its customers and end-users to use such products to infringe the '158 patent.

29. On information and belief, even though Defendant has been aware of the '158 patent, Defendant has not made any changes to the functionality, operations, marketing, sales, technical support, etc. of such products to avoid infringing the '158 patent. Nor has Defendant informed its customers or end-users how to avoid infringing the '158 patent.

30. On information and belief, Defendant itself is unaware of any legal or factual basis that its actions solely, or in combination with the actions of its customers and end-users, do not constitute direct or indirect infringement of the '158 patent.

31. As such, on information and belief, despite the information Defendant obtained from analyzing the '158 patent when responding to an Office Action, Defendant continues to specifically intend for and encourage its customers and end-users to use its products in a manner that infringe the claims of the '158 patent.

32. Defendant's actions of, *inter alia*, making, importing, using, offering for sale, and/or selling such products constitute an objectively high likelihood of infringement of the '158 patent, which was duly issued by the United States Patent and Trademark Office and is presumed valid. Since at least when it received the October 4, 2006 Office Action, Defendant is aware that there is an objectively high likelihood that its actions constituted, and continue to constitute, infringement of the '158 patent and that the '158 patent is valid. Despite Defendant's knowledge of that risk, on information and belief, Defendant has not made any changes to the relevant operation of its products and has not provided its users and/or customers with instructions on how to avoid infringement the '158 patent. Instead, Defendant has continued to, and still is continuing to, among other things, make, use, offer for sale, and/or sell products patented under the '158 patent. As such, Defendant willfully, wantonly and deliberately infringed and is infringing the '158 patent in disregard of

QuickCompile's rights under the '158 patent.

33. QuickCompile is entitled to recover from Defendant the damages sustained by QuickCompile as a result of Defendant's infringement of the '158 patent in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,587,699

34. QuickCompile repeats and realleges the allegations of paragraphs 1 through 33 as if fully set forth herein.

35. Without license or authorization and in violation of 35 U.S.C. § 271(a), Defendant has infringed and continues to infringe at least claims1, 2 and 4-5 of the '699 patent by making, using, importing, offering for sale, and/or selling a system for programming FPGAs, including but not limited to Xilinx Vivado HLS.

36. More specifically and upon information and belief, Vivado HLS accepts algorithms specified in source code of high level languages, such as C, and C++, *see* http://www.xilinx.com/products/design-tools/vivado/integration/esl-design.html (last accessed May 21, 2015), and it supports processing data vectors. *See* Introduction to FPGA Design with Vivado High-Level Synthesis at 42 (available at http://www.xilinx.com/support/documentation/sw_manuals/ug998-vivado-intro-fpga-design-hls.pdf (last accessed May 21, 2015)); *see also* Zynq-7000 All Programmable SoC Accelerator for Floating-Point Matrix Multiplication using Vivado HLS at 2 (available at http://www.xilinx.com/support/documentation/application_notes/xapp1170-zynq-hls.pdf (last accessed May 21, 2015)). The Vivado HLS compiler analyzes the input source code and identifies vector processing operations. *See* Introduction to FPGA Design with Vivado High-

Level Synthesis at 32 (available at http://www.xilinx.com/support/documentation/sw_manuals/ug998-vivado-intro-fpga-design-hls.pdf (last accessed May 21, 2015)); *see also* Vivado Design Suite User Guide: High-Level Synthesis at 85, 87 (available at http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug902-vivado-high-level-synthesis.pdf (last accessed May 21, 2015)). It maps the vector processing operations onto the hardware resources of an FPGA. *See* Zynq-7000 All Programmable SoC Accelerator for Floating-Point Matrix Multiplication using Vivado HLS at 3 (available at http://www.xilinx.com/support/documentation/application_notes/xapp1170-zynq-hls.pdf (last accessed May 21, 2015)); *see also see also* Vivado Design Suite User Guide: High-Level Synthesis at 7 (available at http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug902-vivado-high-level-synthesis.pdf (last accessed May 21, 2015)); Introduction to FPGA Design with Vivado High-Level Synthesis at 51 (available at http://www.xilinx.com/support/documentation/sw_manuals/ug998-vivado-intro-fpga-design-hls.pdf (last accessed May 21, 2015)). The Vivado HLS outputs a hardware design, which is used to program an FPGA with the user's algorithm. *See* Vivado Design Suite User Guide: High-Level Synthesis at 5, 12, 13 (available at http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_1/ug902-vivado-high-level-synthesis.pdf (last accessed May 21, 2015)); *see also* Zynq-7000 All Programmable SoC Accelerator for Floating-Point Matrix Multiplication using Vivado HLS at 3 (available at http://www.xilinx.com/support/documentation/application_notes/xapp1170-zynq-hls.pdf (last accessed May 21, 2015))

37. QuickCompile is entitled to recover from Defendant the damages sustained by QuickCompile as a result of Defendant's infringement of the '699 patent in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

QuickCompile hereby demands a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, QuickCompile requests that this Court enter judgment against Defendant as follows:

A. An adjudication that Defendant has infringed the '158 and '699 patents;

B. A judgment that Defendant has induced infringement of the '158 patent;

C. An award of damages to be paid by Defendant adequate to compensate QuickCompile for Defendant's past infringement of the '158 and '699 patents and any continuing or future infringement through the date such judgment is entered, including interest, costs, expenses and an accounting of all infringing acts including, but not limited to, those acts not presented at trial;

D. A declaration that this case is exceptional under 35 U.S.C. § 285, and an award of QuickCompile's reasonable attorneys' fees;

E. An award of enhanced damages pursuant to 35 U.S.C. § 284 for Defendant's willful infringement of the '158 patent subsequent to the date of its notice of the '158 patent; and

F. An award to QuickCompile of such further relief at law or in equity as the Court deems just and proper.

Dated: May 22, 2015

/s/ Andrew W. Spangler

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